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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,646	10/16/2001	Anthony Debling	S1022/8762	7546

23628 7590 07/22/2004

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EXAMINER	
MCCARTHY, CHRISTOPHER S	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 07/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/981,646	DEBLING, ANTHONY	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/16 &; 12/17/01/*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: The title is in conflict with co-pending application 09/981,646, which has the same title. One or both titles should be changed. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Swoboda U.S. Patent Application Publication US2002/0059541.

As per claim 1, Swoboda teaches an integrated circuit chip comprising embedded digital processor (paragraph 0031, 0069) and an on-chip emulation device coupled to said digital signal processor, said emulation device being operable to control said digital processor and to collect information about the operation of said digital processor (paragraph 0061, 0055), the on-chip emulation device having a communication port for off-chip communication (paragraph 0061,

0038, 0080), the chip further comprising an on-chip interface having a first port connected to said communication port of said on-chip emulation device (paragraph 0080) and a second port for connection to a non-proprietary bus (paragraph 0080) wherein said interface is operable to convert between a format suitable for said on-chip emulation device and a format suitable for said non-proprietary bus (paragraph0080, 0064, 0066).

As per claim 2, Swoboda teaches the integrated circuit chip of claim 1 having plural embedded digital processors, each having a respective associated on-chip emulation device and a respective said on-chip interface, said integrated circuit chip further including said non-proprietary bus, and a bus connection port connected on said chip via said non-proprietary bus to the second port of each said interface (paragraph 0082).

As per claim 3, Swoboda teaches the integrated circuit chip of claim 1 wherein said non-proprietary bus is a universal serial bus (paragraph 0066).

As per claim 4, Swoboda teaches the integrated circuit chip of claim 3 wherein said bus connection port is a universal serial bus hub (paragraph0066, 0039, wherein, it is inherent with multiple connections, which could be multiple USB connections, that a hub be used to control the co-existing connections).

As per claim 5, Swoboda teaches the integrated circuit chip of claim 1 wherein said non-proprietary bus is a bus complying with IEEE standard 1394 (paragraph 0067).

As per claim 6, Swoboda teaches the integrated circuit chip of claim 1 wherein the or each digital processor further comprises JTAG circuitry connected to said bus (paragraph 0062).

As per claim 7, Swoboda teaches the integrated circuit chip of claim 6 wherein said JTAG circuitry has a further off-chip connection (paragraph 0069).

As per claim 8, Swoboda teaches a method of communicating between a remote device and a digital processor (paragraph 0031, 0060, 0038), said digital processor being on an integrated circuit chip (paragraph 0069), said chip having on-chip emulation circuitry for monitoring and controlling the digital processor in response to signals from a said remote device (paragraph 0081), said chip further comprising interface circuitry disposed between a port of said on-chip emulation circuitry and a communication port for said signals (paragraph 0080, wherein, the circuitry is inherent in the port driver interface), wherein said port is adapted to receive a non-proprietary bus and wherein said non-proprietary bus is adapted to convey signals having a predetermined protocol (paragraph 0080, 0064, 0066, wherein, the protocol is inherent in the proper communication of a USB connection), the method comprising: connecting said non-proprietary bus to said port and to a said remote device (paragraph 0080); receiving said signals from said remote device over said non-proprietary bus in said non-proprietary protocol at said communication port and transferring said signals to said interface circuitry on-chip (paragraph 0080, 0064, 0066); in said interface circuitry, converting said signals into a form suitable for said on-chip emulation circuitry, and transferring said converted signals to said on-chip emulation circuitry whereby said on-chip emulation circuitry responds to said converted signals to monitor and control said digital processor (paragraph 0080, 0064, 0066, 0039, 0060).

As per claim 9, Swoboda teaches a method of debugging a digital processor using a host computer, said digital processor being on an integrated circuit chip (paragraph 0031, 0060, 0038, 0069), said chip having on-chip emulation circuitry for monitoring and controlling the digital processor in response to signals from said host computer (paragraph 0081, 0080), said chip further comprising interface circuitry disposed between a port of said on-chip emulation circuitry

and a communication port for said signals (paragraph 0080), wherein said port is adapted to receive a non-proprietary bus and wherein said non-proprietary bus is adapted to convey signals having a predetermined protocol (paragraph 0080, 0064, 0066), the method comprising: connecting said non-proprietary bus to said port and to a said host computer (paragraph 0080, 0064, 0066); generating said signals in said host computer (paragraph 0039, 0060); receiving said signals from said host computer over said non-proprietary bus in said non-proprietary protocol at said communication port and transferring said signals to said interface circuitry on-chip (paragraph 0039, 0060, 0066, 0064); in said interface circuitry, converting said signals into a form suitable for said on-chip emulation circuitry, and transferring said converted signals to said on-chip emulation circuitry whereby said on-chip emulation circuitry responds to said converted signals to monitor and control said digital processor (0081, 0039, 0060, 0064, 0066).

As per claim 10, Swoboda teaches the method of claim 8 wherein said chip further comprises peripheral circuitry, and said on-chip emulation circuitry is linked to said peripheral circuitry for control and monitoring thereof (paragraph 0069).

As per claim 11, Swoboda teaches the method of claim 8 wherein said non-proprietary bus is a universal serial bus and said predetermined protocol is a universal serial bus protocol (paragraph 0064, 0066, wherein, the protocol of USB is inherent in the use of the USB connection).

As per claim 12, Swoboda teaches the method of claim 11 wherein said integrated circuit chip further comprises JTAG circuitry connected to said interface circuitry, the method further comprising supplying test signals over said universal serial bus to said interface circuitry; in said interface circuitry converting said test signals into JTAG protocol form; and supplying said

JTAG protocol signals to said JTAG circuitry whereby said JTAG circuitry implements boundary test functions of said chip (paragraph 0080 – 0082).

As per claim 13, Swoboda teaches the method of claim 12 further comprising causing said on-chip emulation circuitry to determine data illustrative of the behavior of said chip said signals comprise interrogating signals for said on-chip emulation circuitry, whereby said on-chip emulation circuitry derives information from said data to said interface; in said interface, converting said information into universal serial bus protocol; and transmitting said information in universal serial bus protocol over said universal serial bus to said host (paragraph 0080–0082).

Allowable Subject Matter

4. Claims 14-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Double Patenting

5. Claims 1, 3, 8, 9, and 11 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 3 of U.S. Patent Application No. 09/981,624. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

As per claim 1, the present application (referred to hereon as 646) recites an integrated circuit chip comprising embedded digital processor and an on-chip emulation device coupled to said digital signal processor, said emulation device being operable to control said digital

processor and to collect information about the operation of said digital processor. These limitations are taught by application 09/981,624 (referred to hereon as 624, and is italicized for clarity) in claim 3 as it recites a *method of debugging an integrated circuit chip by communicating between application programs running on a host computer system and a device on said integrated circuit chip, the chip comprising digital processing circuitry and on-chip emulation circuitry for communicating with and control of said digital processing circuitry.* The present invention further recites the on-chip emulation device having a communication port for off-chip communication, the chip further comprising an on-chip interface having a first port connected to said communication port of said on-chip emulation device and a second port for connection to a non-proprietary bus. Application 624 recites *the on-chip emulation circuitry having a communications port for receiving information from said host computer system and for passing information to said host computer system, the integrated circuit chip further having an on-chip usb interface connected to a target usb port, and the host computer system having a host usb port.* Lastly, claim 1 of 646 recites wherein said interface is operable to convert between a format suitable for said on-chip emulation device and a format suitable for said non-proprietary bus. Claim 3 of 624 recites *converting said host usb port to said target usb port; running a proxy server program on said host computer system, causing a said application program to connect to said proxy server program, whereby said proxy server program connects to said device on said chip via said host and target usb ports.* Therefore, all limitations of claim 1 of the present application is taught in claim 3 of application 624. However, claim 1 of the present application teaches these limitations to incur in an apparatus; whereas application 624 teaches, in claim 3, the invention as incurring as a method. "Official Notice" is taken that the method of

624 would be performed upon the apparatus of 646. It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the method of 646 on the apparatus of 624. One of ordinary skill in the art would have been motivated to perform the method of 646 on the apparatus of 624 because the method of 646 would have to be performed upon an apparatus, inherently, and 642 contains the needed components to run the method of 646.

As per claim 3, the present invention of 646 recites the integrated circuit chip of claim 1 wherein said non-proprietary bus is a universal serial bus. This limitation is recited in claim 3 of 624 as *the integrated circuit chip further having an on-chip usb interface connected to a target usb port, and the host computer system having a host usb port*, wherein a USB port inherently implies a universal serial bus connection.

As per claim 8, the present invention of 646 recites a method of communicating between a remote device and a digital processor, said digital processor being on an integrated circuit chip. Application 624 recites *a method of debugging an integrated circuit chip by communicating between application programs running on a host computer system and a device on said integrated circuit chip, the chip comprising digital processing circuitry*. Furthermore, 646 recites said chip having on-chip emulation circuitry for monitoring and controlling the digital processor in response to signals from a said remote device. Application 624 recites *on-chip emulation circuitry for communicating with and control of said digital processing circuitry*. The present application further recites that said chip further comprising interface circuitry disposed between a port of said on-chip emulation circuitry and a communication port for said signals, wherein said port is adapted to receive a non-proprietary bus and wherein said non-proprietary

bus is adapted to convey signals having a predetermined protocol, the method comprising: connecting said non-proprietary bus to said port and to a said remote device. Application 624 recites *on-chip emulation circuitry having a communications port for receiving information from said host computer system and for passing information to said host computer system, the integrated circuit chip further having an on-chip usb interface connected to a target usb port, and the host computer system having a host usb port.* Application 646 recites receiving said signals from said remote device over said non-proprietary bus in said non-proprietary protocol at said communication port and transferring said signals to said interface circuitry on-chip; in said interface circuitry, converting said signals into a form suitable for said on-chip emulation circuitry, and transferring said converted signals to said on-chip emulation circuitry whereby said on-chip emulation circuitry responds to said converted signals to monitor and control said digital processor. Application 624 recites an *on-chip usb interface connected to a target usb port, and the host computer system having a host usb port, the method comprising: converting said host usb port to said target usb port; running a proxy server program on said host computer system, causing a said application program to connect to said proxy server program, whereby said proxy server program connects to said device on said chip via said host and target usb ports.* While application 624 does recite a universal serial bus connection, it does not explicitly recite using a predetermined protocol. "Official Notice" is taken that a predetermined protocol would be used in the USB connection of 624 and, therefore, teaches this limitation. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a predetermined protocol in the method of 624. One of ordinary skill in the art would have been motivated to use a predetermined protocol in 624 because a conforming protocol would need to

be utilized in the USB connection to ensure a proper connection, and choosing a proper protocol before the connection is made would ensure a successful connection upon initial connection.

As per claim 9, the present invention of 646 recites a method of debugging a digital processor using a host computer, said digital processor being on an integrated circuit chip, said chip having on-chip emulation circuitry for monitoring and controlling the digital processor in response to signals from said host computer. Application 624 recites *a method of debugging an integrated circuit chip by communicating between application programs running on a host computer system and a device on said integrated circuit chip, the chip comprising digital processing circuitry and on-chip emulation circuitry for communicating with and control of said digital processing circuitry.* Application 646 further recites said chip further comprising interface circuitry disposed between a port of said on-chip emulation circuitry and a communication port for said signals, wherein said port is adapted to receive a non-proprietary bus and wherein said non-proprietary bus is adapted to convey signals having a predetermined protocol, the method comprising: connecting said non-proprietary bus to said port and to a said host computer. Application 624 recites *the on-chip emulation circuitry having a communications port for receiving information from said host computer system and for passing information to said host computer system, the integrated circuit chip further having an on-chip usb interface connected to a target usb port, and the host computer system having a host usb port.* Furthermore, application 646 recites generating said signals in said host computer; receiving said signals from said host computer over said non-proprietary bus in said non-proprietary protocol at said communication port and transferring said signals to said interface circuitry on-chip; in said interface circuitry, converting said signals into a form suitable for said

on-chip emulation circuitry, and transferring said converted signals to said on-chip emulation circuitry whereby said on-chip emulation circuitry responds to said converted signals to monitor and control said digital processor. Application 624 recites *converting said host usb port to said target usb port; running a proxy server program on said host computer system, causing a said application program to connect to said proxy server program, whereby said proxy server program connects to said device on said chip via said host and target usb ports; and on-chip emulation circuitry having a communications port for receiving information from said host computer system and for passing information to said host computer system, the integrated circuit chip further having an on-chip usb interface connected to a target usb port, and the host computer system having a host usb port.* While application 624 does recite a universal serial bus connection, it does not explicitly recite using a predetermined protocol. "Official Notice" is taken that a predetermined protocol would be used in the USB connection of 624 and, therefore, teaches this limitation. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a predetermined protocol in the method of 624. One of ordinary skill in the art would have been motivated to use a predetermined protocol in 624 because a conforming protocol would need to be utilized in the USB connection to ensure a proper connection, and choosing a proper protocol before the connection is made would ensure a successful connection upon initial connection.

As per claim 11, application 646 recites the method of claim 8 wherein said non-proprietary bus is a universal serial bus and said predetermined protocol is a universal serial bus protocol. Application 624 recites integrated circuit chip further having an on-chip usb interface connected to a target usb port, and the host computer system having a host usb port. While

application 624 does recite a universal serial bus connection, it does not explicitly recite using a predetermined protocol. "Official Notice" is taken that a predetermined protocol would be used in the USB connection of 624 and, therefore, teaches this limitation. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a predetermined protocol in the method of 624. One of ordinary skill in the art would have been motivated to use a predetermined protocol in 624 because a conforming protocol would need to be utilized in the USB connection to ensure a proper connection, and choosing a proper protocol before the connection is made would ensure a successful connection upon initial connection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: See attached PYO-892/

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (703)305-7599. The examiner can normally be reached on M-F, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703)305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

csm
July 19, 2004

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